# V6067

## 3U VPX Versal® Premium ASoC FPGA + Ethernet Offload Optical I/O Module with QMC Site

## Benefits

Heterogeneous computing card combining hard ARM processor cores, AI/ML engines, and high-bandwidth networking

Designed specifically for sensor interfaces, data processing, and data distribution in VPX systems

Programmable interface solution that leverages off-the-shelf world-class network performance with customizable application processor and data distribution

HPEC focus, 3U VPX, VITA 47 compliance, SOSA aligned options

Versatile design supports electrical or optical interfaces, optical options for both backplane or front-panel I/O

Modular optics for flexibility in supporting 1-25Gbs per lane

## Features

Xilinx® Versal® ASoC (FPGA): VP1502/VP1702

NVIDIA® Mellanox® ConnectX®-7 Network Interface Device, Hardware offloads for UDP, TCP, RoCE v2, DPDK, GPUDirect, NVMEoF, +more

Up to twenty four (24) 1G to 25G optical ports via MPO front panel I/O or VITA 66 optical backplane I/O

3 banks of 16GB (48 GB total) up to 1866MHz/3733Mbs

PCIe Gen4 support

VITA 93 QMC site with routing to Versal® as PCIE or high-speed serial

Thermal sensors for monitoring card temperature

Robust FPGA example design

Petalinux BSP

Hard silicon MACSEC implementation in MC-X7 and Versal ASoC (FPGA) device

## Overview

The V6067 is a next generation high-performance embedded computing 3U VPX module featuring the Xilinx® Versal® Premium Adaptive System-on-Chip (ASoC), the NVIDIA® Mellanox® ConnectX®-7 (MC-X7) network interface device, rugged optical and electrical I/O, and SOSA aligned profile options. The V6067 is specifically targeted at applications requiring a combination of high- speed data interfaces, network protocol offloads, onboard processing resources, and optional data distribution to adjacent processing resources (CPUs/ GPUs) in the system.

The V6067 is a proven high-bandwidth and low-latency performance leader in 10/25/40/50/100Gbs Ethernet applications. Use cases include sensor interfacing, data processing, data distribution, and FPGA co-processing applications. Radar, signals intelligence, electronic warfare, video, storage, medical imaging, and embedded communications systems all can benefit from the V6067 module. The V6067 includes hardware offloads for UDP, TCP, RoCE v2, DPDK, GPUDirect, NVMEoF, among many other protocol stacks, and excels at high-bandwidth interface applications where data can be processed locally and/or distributed efficiently across the VPX backplane.

The combination of the MC-X7 device and the ASoC device allows for system designers to leverage the off-the-shelf world-class Ethernet performance of the MC-X7 while deploying unique data processing and security algorithms in the onboard ASoC device. This combination maximizes the effectiveness of the deployed applications and algorithms while eliminating design efforts required to establish truly high-bandwidth and low-latency Ethernet, PCIe controllers, PCIe switches, efficient DMA engines, or low overhead software drivers. Hard silicon MACSEC in both the MC-X7 and Versal® Premium gives designers great flexibility implementing datapath security features.

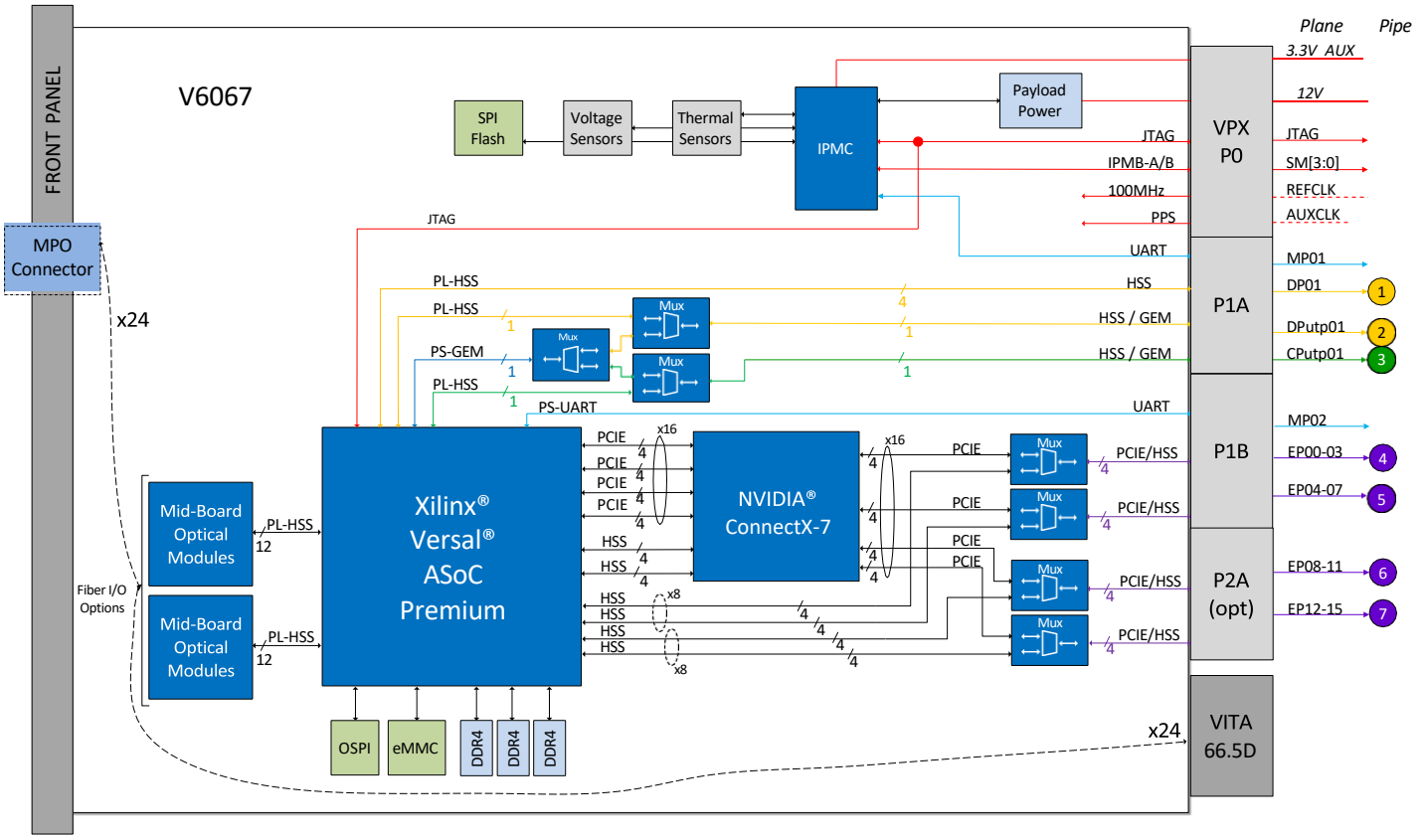
In addition to the Ethernet interfaces described, the FPGA fabric provided within the ASoC part is capable of hosting New Wave IP cores for Fibre Channel, ARINC-818, sFPDP, Aurora, and others. This makes the V6067 an ideal hardware platform for mixed interface protocol needs or protocol bridging applications.

The V6067 is a standout sensor interface and heterogeneous computing solution whether used standalone or adjacent to other processing elements.

The inclusion of a VITA93 QMC site enables customization and flexibility to meet application specific requirements such as NVMe storage or additional AI accelerator functionality. Further, this configuration scalability and future QMC module upgrades to increase performance or add new functionalities long into the products life.

# V6067

## 3U VPX Versal® Premium ASoC FPGA + Ethernet Offload Optical I/O Module




SOSA Plane Legend

| | | | | | |
|---|---|---|---|---|---|
| CP | Control Plane | EP | Expansion Plane | UP | Utility Plane |
| DP | Data Plane | MP | Maintenance Plane | | |

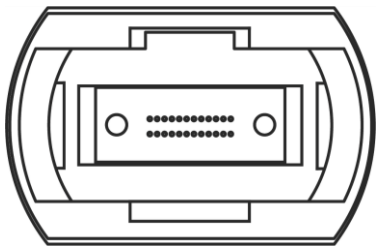
*> V6067 Block Diagram*

## Optical Connector Options

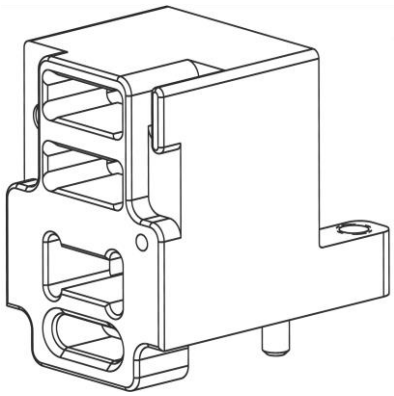
The V6061 offers three different optical I/O options:

1. Optical Front Panel MPO Connector
2. Optical Backplane MT Connector for VITA 66.5
3. No optics

1. Front Panel MPO (Female) I/O



2. VITA 66.5 Backplane MT I/O 1



1Termination: VITA 66.5 Style D (pictured)

# V6067

## 3U VPX Versal® ASoC FPGA + Ethernet Offload Optical I/O Module

## Multi-Processor Multi-Core Support

The V6067 is uniquely suited for system architectures involving multiple processing cards on a common switched data plane. Specifically, the V6067 supports shared access from multiple host processors, enabling it to function as a cost-effective, high-performance gateway. This feature enables a single high-speed pipe to carry multiple virtual channels in systems that need to spread or load-balance sensor data across processor arrays.

## Complete Product Support Program

New Wave prides itself on its excellent customer support, a fact that is echoed by our customers. New Wave DV provides industry standard warranty on its products, but it is the human factor that makes our support so valuable to our customers. Our team takes the time and effort to ensure that the customer experience with our products is a positive one.

## Our Commitment

New Wave is committed to providing the latest innovations in technology, architectures, and techniques to keep our customers one step ahead of the rest. Our products, complete with the Development Framework, are intended to offer our customers an entirely unique out-of-the-box experience.

## Technical Specifications

**PHYSICAL CHARACTERISTICS**

**Dimensions:**

170.75mm length: Face of carrier to back edge of Guide pin connectors
189.22mm length: MPO flip door to back edge of Guide pin connectors
100mm width: Edge of guide rail to guide rail

24.64mm height: From primary cover to secondary cover

**Weight:**

<1.764 lbs (800g)

**POWER CHARACTERISTICS**

Power Draw (Max): 216W
Cooling Capability in 48.2 ECC4 C2 (85° C): 150W
Power Supply: 12V

**TEMPERATURE**

Operating: -40˚ C to 85˚ C (conduction-cooled)
Storage: -55˚ C to 105˚ C

## Technical Specifications

**NETWORK INTERFACE**

Up to twenty four (24) 1G to 25G optical ports (front & backplane options)
- 850nm multi-mode optics

22 lanes of electrical high-speed network IO available to backplane

**ETHERNET PROTOCOLS**

TCP, UDP, ARP, ICMP, RoCEv2, Multicast, Broadcast, + more
Visit NVIDIA® Mellanox® Datasheet1

**OPTIONAL ADDITIONAL PROTOCOLS**

Fibre Channel, sFPDP, ARINC 818, Aurora

**ASoC (FPGA) DEVICE**

Xilinx® Versal® VP1502, VP1702
Visit Xilinx® Versal® Datasheet3

**ETHERNET DEVICE**

NVIDIA® Mellanox® ConnectX®-7 EN IC
Visit NVIDIA® Mellanox® Datasheet1

**MEMORY**

3 banks of 16GB (48GB total) up to 1866MHz/3733Mbs LPDDR4 SDRAM

**PCIe INTERFACE**

One PCI Express Gen4x16 Interfaces over Expansion Plane or
Two PCI Express Gen4x8 Interfaces over Expansion Plane

**THERMAL SENSORS**

2 digital temperature sensors

**COMPLIANCE**

VITA 47, 48.2, 65, 66.5
NVIDIA® Mellanox® ConnectX®-7 EN IC
Visit NVIDIA® Mellanox® Datasheet1

**SOFTWARE SUPPORT**

Software drivers available from NVIDIA® Mellanox®2
NWDV Maintained x86 OS's:
https://newwavedv.com/wordpress/wp-content/uploads/2022/11/V6061-Software-Info.pdf

*This hardware can also support InfiniBand.*

*Please reach out for more information.*

1NVIDIA® Mellanox® ConnectX®-5 EN IC Datasheet: https://newwavedv.com/wordpress/wp-content/uploads/2023/01/pb_connectx-5_en_ic.pdf

2NVIDIA® Mellanox® Ethernet Software Support/Datasheet: https://developer.nvidia.com/networking/ethernet-software

3Xilinx® Versal® ASoC Datasheet: https://www.xilinx.com/products/silicon-devices/acap/versal.html

# V6067 Hardware Part Number Configuration

| 400 | - | 06067 | - | "WXYZ" | - | "IP" | - | "CC" |
|---|---|---|---|---|---|---|---|---|
| Series | | Model | | Board Configuration | | IP Configuration | | Coating Configuration |
| | | | | Select 1 for each W, X, Y, and Z | | Select 1 IP Option | | Optional<br>Select 1 Coating Option |

400-06067-W X Y Z - IP - CC

## W

| Config # | Description |
|---|---|
| *2+* | *Reserved* |
| **1** | Xilinx Versal VP1702 ASoC |
| **0** | Xilinx Versal VP1502 ASoC |

## Y

| Config # | Description |
|---|---|
| **0** | Conduction cooled, 1" pitch |

## Z

| Config # | Description |
|---|---|
| *3+* | *Reserved* |
| **2** | Industrial Temp |
| *1* | *Reserved* |
| **0** | Commercial Temp |

## IP

| Config # | Description |
|---|---|
| 03+ | Reserved |
| 02 | Example design package, Versal root complex, CX7 multi-host |
| *01* | *Reserved* |
| 00 | Example design package, Versal endpoint, CX7 single host |

## CC

| Config # | Description |
|---|---|
| AR | Acrylic conformal coat |
| UR | Urethane conformal coat |
| ER | Epoxy conformal coat |
| SR | Silicone conformal coat |
| XY | Parylene conformal coat |
| BLANK | No conformal coat |

## X

| Config # | Slot Profile Description | VITA 65 Compatible Profile | VITA 65 Aperture Style |
|---|---|---|---|
| *I+* | *Reserved* | *n/a* | *n/a* |
| H | No optics populated, P2A not populated with single-wide QMC site | 14.6.11-0 | J* |
| G | 24 lane1-25Gbps front panel MPO optics, P2A not populated | 14.6.11-0 | J* |
| F | 12-lane 1-25Gbps front panel MPO optics, P2A not populated with single-wide QMC site | 14.6.11-0 | J* |
| E | 24-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated | 14.6.11-14 | J* |
| D | 12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated with single-wide QMC site | 14.6.11-14 | J* |
| C | 16-lane 1-25Gbps front panel MPO optics, P2A not populated | 14.6.11-0 | J* |
| B | 8-lane 1-25Gbps front panel MPO optics, P2A not populated with single-wide QMC site | 14.6.11-0 | J* |
| A | 16-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated | 14.6.11-14 | J* |
| 9 | 8-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated with single-wide QMC site | 14.6.11-14 | J* |
| 8 | No optics populated, P2A populated with single-wide QMC site | 14.6.13-0 | J |
| 7 | 24-lane 1-25Gbps front panel MPO optics, P2A populated | 14.6.13-0 | J |
| 6 | 12-lane 1-25Gbps front panel MPO optics, P2A populated with single-wide QMC site | 14.6.13-0 | J |
| 5 | 24-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated | 14.6.13-8 | J |
| 4 | 12-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated with single-wide QMC site | 14.6.13-8 | J |
| 3 | 16-lane 1-25Gbps front panel MPO optics, P2A populated | 14.6.13-0 | J |
| 2 | 8-lane 1-25Gbps front panel MPO optics, P2A populated with single-wide QMC site | 14.6.13-0 | J |
| 1 | 16-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated | 14.6.13-8 | J |
| 0 | 8-lane 1-25Gbps backplane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated with single-wide QMC site | 14.6.13-8 | J |

*14.6.11 Specifies an H style aperture with 2 style C fiber connectors, or an alternative style connector(s) that fit with the aperture space. 14.6.11 options 9, A, D, and E and 14.6.13 options 0, 1, 4 and 5 are delivered with a single style D connector thus meeting the specification of Style H or Style J.

# V6067 “Go-Fast” Hardware Part Numbers

*Configurations below are available with the shortest lead times.*

| Config # | Configuration Description |
|---|---|
| **“.11” Profiles** | |
| **400-06067-1A02-00** | V6067 FPGA + Ethernet NIC 3U VPX Module, Xilinx Versal VP1702 ASoC, 16-lane 1-25Gbps back-plane VITA 66 optics MTB-MM24-6.5.3.5, P2A not populated, conduction cooled, 1” pitch, sin- gle-host, industrial temp, example design package |
| **400-06067-1H02-00** | V6067 FPGA + Ethernet NIC 3U VPX Module, Xilinx Versal VP1702 ASoC, optics not populated, P2A not populated, conduction cooled, 1” pitch, industrial temp, single-host, example design package |

| “.13” Profiles | |
|---|---|
| **400-06067-1102-00** | V6067 FPGA + Ethernet NIC 3U VPX Module, Xilinx Versal VP1702 ASoC, 16-lane 1-25 Gbps back-plane VITA 66 optics MTB-MM24-6.5.3.5, P2A populated, conduction cooled, 1” pitch, industrial temp, single-host, example design package |
| **400-06067-1802-00** | V6067 FPGA + Ethernet 3U VPX Module, Xilinx Versal VP1702 ASoC, optics not populated, P2A popu-lated, conduction cooled, 1” pitch, industrial temp, single-host, example design package |

FOR MORE INFORMATION
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